IN THE SPECIFICATION:

Kindly replace the paragraph beginning on page 2, line 15, with the following:

The present invention is related to the following commonly-assigned, copending applications:

"LDPC Encoder and Method Thereof", filed on even date and assigned application Serial No. 09/730,752 (Attorney Docket No. MP0064), the contents of which are incorporated herein by reference,

"Address Generator for LDPC Encoder and Decoder and Method Thereof" filed on even date and assigned application Serial No. 09/730,597 (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference, and

"Parity Check Matrix and Method of Forming Thereof", filed on even date and assigned application Serial No. 09/730,598 (Attorney Docket No. MP0069), the contents of which are incorporated herein by reference.

Kindly replace the paragraph beginning on page 3, line 10, with the following:

The operation of transmission section 300 will now be explained. Prior to processing by transmitting section 300, input or user data maybe encoded with an error correcting code, such as the Reed/Solomon code, or run length limited encoded (RLL) or a combination thereof by encoder 302. The encoded output encoder 302 is then interleaved by deinterleaver 308 for input to linear block code encoder 304 which generates parity data in a known manner utilizing linear block codes. One example of a linear block code is a low-density parity-check code (LDPC) which is discussed by Robert G. Gallager in *Low-Density Parity-Check Codes*, 1963, M.I.T. Press and by Zining Wu in *Coding and Iterative Detection For Magnetic Recording Channels*, 2000, Kluwer Academic Publishers, the contents of each of which are incorporated in their entirety by reference. Deinterleaver 308 permutes the data so that the same data is reordered before encoding by linear block code encoder 304. By permuting or redistributing the data, ~~interleaver~~ deinterleaver ~~306~~ 308 attempts to reduce the

number of nearest neighbors of small distance error events. User data at the output of encoder 302 is referred to as being in the channel domain; that is the order in which data is transmitted through the channel. The order of data processed by deinterleaver 308 is referred to as being in the linear block code domain. The parity data from linear block code encoder 304 is combined with the data encoded by encoder 302 by multiplexer 306 for input to channel transmitter 310.

Kindly replace the paragraph beginning on page 3, line 29, with the following:

Transmitter 310 transmits the combined user and parity data from multiplexer 306 typically as an analog signal over communication channel 401 in the channel domain. Communication channel 401 may include any wireless, wire, optical and the like communication medium. Receiver 500 comprises a front-end circuit 502 comprising analog to digital and equalization circuits. The digital signal front-end circuit 502 is input to soft channel decoder 504, which provides probability information of the detected data. Soft channel decoder 504 may be implemented by a Soft Viterbi Detector or the like. The output of the soft channel decoder 504, which is in the channel domain, is converted into the linear block code domain by deinterleaver 510. Deinterleaver 510 is constructed similarly to deinterleaver 308. Soft linear block code decoder 506 utilizes this information and the parity bits to decode the received data. One output of soft linear block code decoder 506 is fed back to soft channel decoder 504 via interleaver 512, which converts data in the linear block code domain to the channel domain. ~~Deinterleaver~~ Interleaver 512 is constructed to perform the reverse operations of deinterleaver 510. Soft channel decoder 504 and soft linear block code decoder 506 operate in an iterative manner to decode the detected data.

Kindly replace the paragraph beginning on page 4, line 14, with the following:

The other output of soft linear block code decoder 506 is converted from the linear block domain to the channel domain by interleaver 514. ~~Deinterleaver~~ Interleaver 514 is constructed similarly to interleaver 512. The output of interleaver 514 is passed on for

further processing to decoder 508. Decoder 508 is implemented to perform the reverse operations of encoder 302.

Kindly replace the paragraph beginning on page 5, line 9, with the following:

According to a fifth aspect of the present invention, the method further comprises the steps of (g) converting ~~|LLrAPP$_k$|~~ |LLrAPP$_l$| information into hard information ~~$b_{e,k}$~~ $b_{c,l}$, (h) calculating an equation syndrome for each parity check equation, s_i. (i) summing each of equation syndrome in step h, (j) outputting the hard information if the sum in step i is equal to zero; (k) repeating steps a-c if the sum in step i is not equal to zero, (l) determining if *i* is less than a first predetermined value; (m) repeating steps a-c, if in step l, *i* is less than the first predetermined value; (n) determining if the sum in step i is less than a second predetermined value; and (o) outputting the hard information if *i* is at least the first predetermined and the sum in step i is less than the second predetermined value.

Kindly replace the paragraph beginning on page 5, line 19, with the following:

According to a sixth aspect of the present invention, the method further comprises the steps of (p) for each data [[*k*]] *l*, determining if ~~|LLrAPP$_k$|~~ |LLrAPP$_l$| is less than a third predetermined value; (q) for each data [[*k*]] *l*, outputting hard information ~~$b_{e,k}$~~ $b_{c,l}$ if ~~|LLrAPP$_k$|~~ |LLrAPP$_l$| is at least the third predetermined value; and (r) for each data [[*k*]] *l*, outputting soft channel information ~~$b_{s,k}$~~ $b_{s,l}$ if ~~|LLrAPP$_k$|~~ |LLrAPP$_l$| is less than the third predetermined value.

Kindly replace the paragraph beginning on page 6, line 3, with the following:

According to a seventh aspect of the present invention, the method further comprises the steps of (s) for each data [[k]] l, determining if a corresponding parity check equation is violated, (t) for each data [[k]] l, outputting hard information ~~$b_{e,k}$~~ $b_{c,l}$, if the corresponding parity check equation is not violated, (u) for each data [[k]] l, determining if ~~$|LLrAPP_k|$~~ $|LLrAPP_l|$ is less than a third predetermined value, (v) for each data [[k]] l, outputting hard information ~~$b_{e,k}$~~ $b_{c,l}$ if ~~$|LLrAPP_k|$~~ $|LLrAPP_l|$ is at least the third predetermined value, and (w) for each data [[k]] l, outputting soft channel information ~~$b_{s,k}$~~ $b_{s,l}$ if ~~$|LLrAPP_k|$~~ $|LLrAPP_l|$ is less than the third predetermined value.

Kindly replace the paragraph beginning on page 7, line 6, with the following:

According to a twelfth aspect of the present invention, the computer program further comprises the steps of (g) converting ~~$|LLrAPP_k|$~~ $|LLrAPP_l|$ information into hard information ~~$b_{e,k}$~~ $b_{c,l}$, (h) calculating an equation syndrome for each parity check equation, s_i. (i) summing each of equation syndrome in step h, (j) outputting the hard information if the sum in step i is equal to zero; (k) repeating steps a-c if the sum in step i is not equal to zero, (l) determining if i is less than a first predetermined value; (m) repeating steps a-c, if in step l, i is less than the first predetermined value; (n) determining if the sum in step i is less than a second predetermined value; and (o) outputting the hard information if i is at least the first predetermined and the sum in step i is less than the second predetermined value.

Kindly replace the paragraph beginning on page 7, line 16, with the following:

According to a thirteenth aspect of the present invention, the computer program further comprises the steps of (p) for each data [[k]] l, determining if ~~$+LLrAPP_k+$~~ $|LLrAPP_l|$ is less than a third predetermined value; (q) for each data [[k]] l, outputting hard information ~~$b_{e,k}$~~ $b_{c,l}$ if ~~$+LLrAPP_k+$~~ $|LLrAPP_l|$ is at least the third predetermined value; and (r) for each data [[k]] l, outputting soft channel information ~~$b_{s,k}$~~ $b_{s,l}$ if ~~$+LLrAPP_k+$~~ $|LLrAPP_l|$ is less than the third predetermined value.

Kindly replace the paragraph beginning on page 7, line 21, with the following:

According to a fourteenth aspect of the present invention, the computer program further comprises the steps of (s) for each data [[k]] l, determining if a corresponding parity check equation is violated, (t) for each data [[k]] l, outputting hard information ~~$b_{e,k}$~~ $b_{c,l}$, if the corresponding parity check equation is not violated, (u) for each data [[k]] l, determining if ~~$+LLrAPP_k+$~~ $|LLrAPP_l|$ is less than a third predetermined value, (v) for each data [[k]] l, outputting hard information ~~$b_{e,k}$~~ $b_{c,l}$ if ~~$+LLrAPP_k+$~~ $|LLrAPP_l|$ is at least the third predetermined value, and (w) for each data [[k]] l, outputting soft channel information ~~$b_{s,k}$~~ $b_{s,l}$ if ~~$+LLrAPP_k+$~~ $|LLrAPP_l|$ is less than the third predetermined value.

Kindly replace the paragraph beginning on page 9, line 11, with the following:

According to a twenty-second aspect of the present invention, the decoder further comprising slicing means for converting ~~$+LLrAPP_k+$~~ $|LLrAPP_l|$ information into hard information ~~$b_{e,k}$~~ $b_{c,l}$; equation vector means for calculating an equation syndrome for each parity check equation s_i, summing means for summing each equation syndrome calculated by

the equation vector means. The hard information is output if the sum by the summing means is equal to zero, and the calculations by the first and second calculating means are repeated if the sum summed by the summing means is not equal to zero.

Kindly replace the paragraph beginning on page 9, line 27, with the following:

According to a twenty-fourth aspect of the present invention, the decoder further comprises third threshold means for determining for each data [[k]] l if ~~$\vert$LLrAPP$_k\vert$~~ $\vert$LLrAPP$_l\vert$ is less than a third predetermined value. For each data [[k]] l, hard information ~~$b_{e,k}$~~ $b_{c,l}$ is output if ~~$\vert$LLrAPP$_k\vert$~~ $\vert$LLrAPP$_l\vert$ is at least the third predetermined value as determined by the third threshold means; and for each data [[k]] l, soft channel information ~~$b_{s,k}$~~ $b_{s,l}$ is output if ~~$\vert$LLrAPP$_k\vert$~~ $\vert$LLrAPP$_l\vert$ is less than the third predetermined value as determined by the third threshold means.

Kindly replace the paragraph beginning on page 10, line 3, with the following:

According to a twenty-fifth aspect of the present invention, the decoder further comprises judging means for determining for each data [[k]] l if a corresponding parity check equation is violated and third threshold means for determining for each data [[k]] l if ~~$\vert$LLrAPP$_k\vert$~~ $\vert$LLrAPP$_l\vert$ is less than a third predetermined value. For each data [[k]] l, hard information ~~$b_{e,k}$~~ $b_{c,l}$, is output if the corresponding parity check equation is not violated as determined by the judging means, for each data [[k]] l, hard information ~~$b_{e,k}$~~ $b_{c,l}$ is output if ~~$\vert$LLrAPP$_k\vert$~~ $\vert$LLrAPP$_l\vert$ is at least the third predetermined value as determined by the third threshold means; and wherein for each data [[k]] l, soft channel information ~~$b_{s,k}$~~ $b_{s,l}$ is output if ~~$\vert$LLrAPP$_k\vert$~~ $\vert$LLrAPP$_l\vert$ is less than the third predetermined value as determined by the third threshold means.

Kindly replace the paragraph beginning on page 11, line 13, with the following:

According to a thirty-third aspect of the present invention, the decoder further comprises a slicer to convert ~~|LLrAPP$_k$|~~ $\underline{|LLrAPP_l|}$ information into hard information ~~$b_{e,k}$~~ $\underline{b_{c,l}}$[[;]], and an equation vector circuit to calculate an equation syndrome for each parity check equation, s_i.

Kindly replace the paragraph beginning on page 12, line 5, with the following:

According to a thirty-sixth aspect of the present invention, the decoder further comprises a third threshold detector to determine for each data [[k]] $\underline{l}$ if ~~|LLrAPP$_k$|~~ $\underline{|LLrAPP_l|}$ is less than a third predetermined value. For each data [[k]] $\underline{l}$, hard information ~~$b_{e,k}$~~ $\underline{b_{c,l}}$ is output if ~~|LLrAPP$_k$|~~ $\underline{|LLrAPP_l|}$ is at least the third predetermined value as determined by the third threshold detector; and for each data [[k]] $\underline{l}$, soft channel information ~~$b_{s,k}$~~ $\underline{b_{s,l}}$ is output if ~~|LLrAPP$_k$|~~ $\underline{|LLrAPP_l|}$ is less than the third predetermined value as determined by the third threshold detector.

Kindly replace the paragraph beginning on page 12, line 12, with the following:

According to a thirty-seventh aspect of the present invention, the decoder further comprises a judging circuit to determine for each data [[k]] $\underline{l}$ if a corresponding parity check equation is violated, and a third threshold detector to determine for each data [[k]] $\underline{l}$ if ~~|LLrAPP$_k$|~~ $\underline{|LLrAPP_l|}$ is less than a third predetermined value. For each data [[k]] $\underline{l}$, hard information ~~$b_{e,k}$~~ $\underline{b_{c,l}}$ is output, if the corresponding parity check equation is not violated as determined by the judging circuit, and for each data [[k]] $\underline{l}$, outputting hard information ~~$b_{e,k}$~~ $\underline{b_{c,l}}$ if ~~|LLrAPP$_k$|~~ $\underline{|LLrAPP_l|}$ is at least the third predetermined value as determined by the

third threshold detector; and for each data [[k]] l, soft channel information ~~$b_{s,k}$~~ $b_{s,l}$ is output if ~~$|LLrAPP_k|$~~ $|LLrAPP_l|$ is less than the third predetermined value as determined by the third threshold detector.

Kindly replace the paragraph beginning on page 14, line 20, with the following:

Referring again to Fig. 2, linear block code encoder 304 utilizes the user data and address from address generator 328 to provide the parity bits to multiplexer 306. Address generator 328 is described in more detail in commonly assigned, copending patent application entitled "Address Generator for LDPC Encoder and Decoder and Method Thereof" filed on even date and assigned application Serial No. 09/730,597 (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference. Linear block code encoder 304 is preferably implemented as a low-density parity-check code (LDPC) encoder as described in commonly assigned, copending patent application entitled "LDPC Encoder and Method Thereof", filed on even date and assigned application Serial No. 09/730,752 (Attorney Docket No. MP0064), the contents of which are incorporated herein by reference. The parity data from linear block code encoder 304 is combined with the data encoded by encoder 302 by multiplexer 306 for input to channel transmitter 310. In the preferred embodiment, the combined data consists of series of a pair parity bits followed by 34 bits of user data. This constraint is established by RLL constraint encoder 302.

Kindly replace the paragraph beginning on page 16, line 11, with the following:

A matrix having 5402 columns can process a maximum LDPC codeword of 5402 bits. Of course, as will be appreciated by one of ordinary skill in the art, the matrix may be truncated to accommodate a smaller block, however the matrix must be at least 222 x 4366 which is dependent on the constraint of encoder 302. This constraint is for example a RLL constraint. The preferred matrix contains no cycles, since a matrix having cycles has degraded performance that degrades significantly. With the first tier only, the parity check matrix has a $D_{min} = 2$; by adding the second tier, the parity check matrix has a $D_{min} = 4$; and

by adding the third tier, the parity check matrix has a $D_{min} = 6$. A further description of the parity check matrix is provided in commonly assigned, copending application entitled, "Parity Check Matrix and Method of Designing Thereof", filed on even date and assigned application Serial No. 09/730,598 (Attorney Docket No. MP0069), the contents of which are incorporated herein by reference.

Kindly replace the paragraph beginning on page 16, line 28, with the following:

A linear code is a set of codewords, **x**, satisfying the matrix equation (1)

$$\mathbf{H} \cdot \mathbf{x} = 0 \qquad (1),$$

where **H** is an **M** x **L** matrix, and **x** is a ~~1 x L~~ L x 1 vector.

Kindly replace the paragraph beginning on page 18, line 14, with the following:

2. Each check equation (each row) calculates the extrinsic information for each involved bit. The "LLRXOR" ($\Sigma \oplus$) denotes the LLR (log-likelihood ratio) operation discussed below.

Kindly replace the paragraph beginning on page 21, line 3, with the following:

2. At each time clock, address generator ~~804~~ 530 calculates the indices of each equation for the current bit, and position index generator 802 calculates the position index thereof. Three $LLrR_{ml}$'s are calculated using Equation 8 by a calculating means or calculator or equation 1 LLR update circuit 816, equation 2 LLR update circuit 818, and equation 3 LLR update circuit 820.

Kindly replace the paragraph beginning on page 22, line 30, with the following:

Fig. 10 is a block diagram of decision circuit 900, and Fig. 14 is a flow chart thereof. Decision circuit 900 is responsive to the output from soft channel decoder ~~914~~ 504, LLrAPP_l from summer or summing means 852 and address generator or address generator means 530. Decision circuit 900 comprises memory 914 for storing hard decision data ~~$b_{s,k}$~~ $b_{s,l}$ (for [[k]] l=1:5402) from soft channel decoder 504, slicer or slicing means 888 for converting $|\mathrm{LLrAPP}_l|$ information into hard information ~~$b_{e,k}$~~ $b_{c,l}$, memory 904 for storing ~~$b_{e,k}$~~ $b_{c,l}$, a threshold detector 902 to determine if $|\mathrm{LLrAPP}_l|$ from summer 852 is less then a threshold value (t_2). Decision circuit or decision means 900 further comprises counter 920 for counting the number of iterations performed by the decoder and threshold detector 910 to determine if the number of iterations exceeds threshold value t_3, which in the preferred embodiment is four. Equation vector circuit or equation vector means 908 determines the equation syndromes, one for each equation, S_m, m=1:222 in which $S_m = 0$ when equation i is satisfied or $S_m = 1$ when equation m is violated. Summer 906 sums each of the S_m, m=1:222.

Kindly replace the paragraph beginning on page 23, line 12, with the following:

The operation of decision circuit 900 will now be explained in conjunction with the flow chart of Fig. 14. After an iteration of iterative decoding, the equation syndrome is calculated by ~~equal~~ equation vector circuit 908 and summed by summer or summing means 906. Threshold circuit 912 determines if the sum of all $S_m = 0$, then a signal is sent to multiplexer 854 to output ~~$b_{e,k}$~~ $b_{c,l}$ from memory 904. If the sum of all $S_m \neq 0$, then a determination is made by threshold detector 910 whether the number of iterations is less than threshold value t_3. If the number of iterations is less than threshold value t_3, the next iteration is performed. Otherwise threshold circuit 912 determines if the sum of all S_m is less than threshold t_1. If so, then a signal is sent to multiplexer 854 to output ~~$b_{e,k}$~~ $b_{c,l}$ from memory 904. Alternatively, the next step in the process is to determine if $|\mathrm{LLrAPP}_l|$ is less then

threshold value (t_2), if so, multiplexer 854 selects ~~$b_{s,k}$~~ $\underline{b_{s,l}}$ to be output. If $|LLrAPP_l|$ is not less then threshold value (t_2), multiplexer 854 selects ~~$b_{e,k}$~~ $\underline{b_{c,l}}$ to be output.

Kindly replace the paragraph beginning on page 23, line 25, with the following:

Fig. 11 is a block diagram of decision circuit 900' and Fig. 15 is a flow chart thereof. Decision circuit 900' is responsive to the output from soft channel decoder ~~914~~ 504, $LLrAPP_l$ from summer 852 and address generator 530. Decision circuit 900' comprises memory 914 for storing hard decision data ~~$b_{s,k}$~~ $\underline{b_{s,l}}$ (for [[k]] $\underline{l}$=1:5402) from soft channel decoder 504, slicer 888 for converting $|LLrAPP_l|$ information into hard information ~~$b_{e,k}$~~ $\underline{b_{c,l}}$, memory 904 for storing ~~$b_{e,k}$~~ $\underline{b_{c,l}}$, a threshold detector 902 to determine if $|LLrAPP_l|$ from summer 852 is less then a threshold value (t_2). Decision circuit 900' further comprises counter 920 for counting the number of iterations performed by the decoder and threshold detector 910 to determine if the number of iterations exceeds threshold value t_3, which in the preferred embodiment is four. Equation vector circuit 908 determines the equation syndromes, one for each equation, S_m, i=1:222 in which $S_m = 0$ when equation i is satisfied or $S_m = 1$ when equation i is violated. Summer 906 sums each of the S_m, m=1:222.

Kindly replace the paragraph beginning on page 24, line 3, with the following:

The operation of decision circuit 900' will now be explained in conjunction with the flow chart of Fig. 15. After an iteration of iterative decoding, the equation syndrome is calculated and summed by ~~equal~~ equation vector circuit 908 and summer 906. Threshold circuit 912 determines if the sum of all $S_m = 0$, then a signal is sent to multiplexer 854 to output ~~$b_{e,k}$~~ $\underline{b_{c,l}}$ from memory 904. If the sum of all $S_m \neq 0$, then a determination is made by threshold detector 910 whether the number of iterations is less than threshold value t_3. If the number of iterations is less than threshold value t_3, the next iteration is performed. Otherwise threshold circuit 912 determines if the sum of all S_m is less than threshold t_1. If so, then a signal is sent to multiplexer 854 to output ~~$b_{e,k}$~~ $\underline{b_{c,l}}$ from memory 904. Alternatively, the next

step in the process is to determine if [[b_k]] b_l is involved in an equation that is violated. If [[b_k]] b_l is not involved in an equation that is violated, multiplexer 854 selects ~~$b_{e,k}$~~ $b_{c,l}$ ~~is provided~~ as the output. Otherwise threshold detector 902 determines if ~~$|LLrAPP_k|$~~ $|LLrAPP_l|$ is less then threshold value (t_2), if so multiplexer 854 selects ~~$b_{s,k}$~~ $b_{s,l}$ to be output. If ~~$|LLrAPP_k|$~~ $|LLrAPP_l|$ is not less then threshold value (t_2), multiplexer 854 selects ~~$b_{e,k}$~~ $b_{c,l}$ to be output.